

Claims

What is claimed is:

1. A portion of circuitry for a circuit comprising an anti-fuse, a first contact pad coupled to a first circuit device, a second contact pad coupled to a second circuit device, wherein said portion comprises a continuous electrical conductor coupled to said first contact pad and said anti-fuse.
2. The portion of circuitry in claim 1, wherein said conductor provides a direct connection between said first contact pad and said anti-fuse.
3. The portion of circuitry in claim 2, wherein said direct connection avoids a channel of any transistor.
4. The portion of circuitry in claim 2, wherein said direct connection avoids a combination of a source and a drain of any particular transistor.
5. The portion of circuitry in claim 2, wherein said conductor is coupled to said second contact pad.
6. The portion of circuitry in claim 5, wherein said conductor is coupled to said second contact pad through a source, a channel, and a drain of a transistor.
7. Circuitry for a semiconductor die, comprising:
 - a first circuit device;
 - a first electrically conductive terminal coupled to said first circuit device;
 - an electrically conductive electrode that is discrete from said circuit device; and
 - an electrically conductive path coupled to said electrically conductive electrode and said first electrically conductive terminal, wherein said path is unregulated by a transistor.

8. The circuitry in claim 7, wherein said electrically conductive electrode is a capacitor plate.
9. The circuitry in claim 8, wherein said capacitor plate is a portion of an anti-fuse.
10. The circuitry in claim 9, wherein said first terminal is configured to couple to at least one voltage source external to said die.
11. The circuitry in claim 9, wherein said first terminal is a first contact pad.
12. A packaged circuit, comprising:
 - a wire;
 - a first pad bonded to said wire;
 - a second pad unbonded to any wire; and
 - a programmable element directly coupled to said second pad and indirectly coupled to said first pad.
13. The packaged circuit in claim 12, further comprising a transistor coupled to said programmable element and said first pad, wherein said transistor is positioned to regulate electrical communication between said programmable element and said first pad.
14. Circuitry for a die, comprising:
 - a first terminal on said die and located to receive a plurality of voltage signals from at least one source external to said die;
 - a second terminal on said die and located to receive a plurality of voltage signals from at least one source external to said die;
 - an anti-fuse; and

a node in unregulated electrical communication with said first terminal and said anti-fuse, said node being in regulated electrical communication with said second terminal.

15. A circuit for a semiconductor die, comprising:

a first pad on said semiconductor die, wherein said first pad is configured to receive at least a first external voltage;
a transistor coupled to said first pad; and
a second pad coupled to said first pad through said transistor, wherein said second pad is configured to receive at least a second external voltage.

16. The circuit in claim 15, further comprising a programming device coupled to said second pad.

17. The circuit in claim 16, wherein said programming device is coupled to said first pad through said transistor.

18. Memory circuitry, comprising:

an equilibration circuit;
a first contact pad coupled to said equilibration circuit;
a memory control circuit;
a second contact pad coupled to said memory control circuit;
an anti-fuse circuit comprising:
a voltage node coupled to said first contact pad,
an anti-fuse coupled to said voltage node,
at least one transistor coupled between said anti-fuse and ground;
a pass gate coupled between said voltage node and said second contact pad; and
a capacitor coupled to said pass gate.

19. The memory circuitry of claim 18, further comprising:

a voltage regulation device coupled to said anti-fuse circuit; and
a latch circuit coupled to said voltage regulation device.

20. Electrical communication devices for programmable circuitry within a packaged part, wherein said part includes a latch circuit and a bonded pad, comprising:

an unbonded pad within said packaged part, wherein said pad is directly coupled to said programmable circuitry; and
a first transistor directly coupled to said programmable circuitry and between said programmable circuitry and said latch circuit.

21. The electrical communication devices in claim 20, further comprising a second transistor directly coupled to said programmable circuitry and between said programmable circuitry and said bonded pad.

22. A computer system, comprising:

a microprocessor;
a clock circuit coupled to said microprocessor; and
a circuit device coupled to said microprocessor and comprising:
a programmable element, and
a conductive terminal directly coupled to said programmable element.

23. The computer system of claim 22, wherein said conductive terminal is electrically isolated from said microprocessor and said clock circuit.

24. The computer system of claim 22, wherein said circuit device is a memory device.

25. The computer system of claim 22, wherein said programmable element is an anti-fuse.

26. A voltage regulation circuit for a programmable element configured to receive a voltage from a node, and a latch circuit configured to read a state of said programmable element, said voltage regulation circuit comprising:

a transistor configured to couple to said latch circuit; and
a first conductive path coupled to said transistor, wherein said first conductive path extends to said node and is interrupted only by said programmable element.

27. The circuit in claim 26, wherein said transistor is an n-channel transistor.

28. The circuit in claim 26, wherein said transistor is a p-channel transistor.

29. The circuit in claim 28, wherein said first conductive path is coupled to a source of said transistor; and wherein said circuit further comprises a second conductive path coupled to a gate of said transistor and extending to said node.

30. The circuit in claim 29, further comprising a multiplexing circuit configured to receive an input, and wherein said second conductive path is interrupted by said multiplexing circuit.

31. A circuit comprising:

an anti-fuse; and
a first contact pad directly coupled to said anti-fuse.

32. The circuit in claim 31, further comprising equilibration circuitry coupled to said first contact pad.

33. The circuit in claim 31, further comprising a second contact pad indirectly coupled to said anti-fuse.

34. The circuit in claim 33, further comprising:
 packaging material over said first contact pad and said second contact pad;
 conductive material extending from said second pad through said packaging material; and
 wherein no conductive material extends from said first contact pad through said packaging material.
35. The circuit in claim 33, further comprising a self-booting pass gate circuit electrically interposed between said second contact pad and said anti-fuse.
36. The circuit in claim 33, further comprising memory write control circuitry coupled to said second contact pad.
37. A method of configuring a semiconductor die, comprising:
 sharing a die terminal between a first device on said die and a second device on said die, wherein said first device is configured to receive a voltage through said die terminal;
 allowing unregulated electrical communication between said die terminal and said second device, wherein an act of determining a status of said second device while said voltage is present at said die terminal may result in an incorrect determination of said status; and
 preventing said act of determining while said voltage is present at said die terminal.
38. The method in claim 37, further comprising:
 including a circuit on said die, wherein said circuit is configured to perform said act of determining; and
 isolating said circuit from said second device while said voltage is present.
39. The method in claim 38, wherein said isolating act comprises:

electrically interposing a transistor between said circuit and said second device;
and
preventing electrical communication between said circuit and said second device
using said transistor.

40. The method in claim 39, wherein said act of preventing electrical communication comprises turning off said transistor in direct response to said voltage being present at said die terminal.

41. The method in claim 40, wherein said sharing act comprises sharing a die terminal between an equilibration circuit and an anti-fuse, wherein said equilibration circuit is configured to receive a margin-testing voltage through said die terminal.

42. A method of protecting a latch circuit from receiving a voltage from a voltage source through an anti-fuse circuit after an anti-fuse-blowing mode of said circuit, said method comprising:

electrically interposing a device between said latch circuit and said anti-fuse circuit, wherein said device is configured to selectively block electrical communication therebetween; and
blocking all electrical communication between said latch circuit and said anti-fuse circuit, wherein said blocking act occurs outside of said anti-fuse-blowing mode and while said voltage is present at said anti-fuse circuit.

43. The method in claim 42, further comprising refraining from interposing any device between said voltage source and said anti-fuse that is configured to selectively block electrical communication therebetween.

44. A method of regulating the voltage transmitted through an anti-fuse to a circuit, said method comprising:

providing a first voltage regulator between said anti-fuse and said circuit, wherein said voltage regulator is configured to discourage electrical communication therethrough when inactivated; and
inactivating said first voltage regulator when a voltage is transmitted to said anti-fuse, wherein no other voltage regulator is present between a first source of said voltage and said anti-fuse.

45. The method in claim 44, further comprising inactivating said first voltage regulator when a voltage is transmitted to said anti-fuse, wherein a second voltage regulator is present between a second source of said voltage and said anti-fuse, and wherein said second voltage regulator allows electrical communication therethrough.

46. The method in claim 45, wherein:

said method further comprises at most partially activating said first voltage regulator when a low voltage is transmitted to said anti-fuse; and
said act of inactivating said first voltage regulator when a voltage is transmitted to said anti-fuse, wherein no other voltage regulator is present between a first source of said voltage and said anti-fuse comprises:
inactivating said first voltage regulator when a high voltage is transmitted.

47. A method of providing voltage to a circuit including a first pad, a second pad, and a programmable element, and a latch, said method comprising:

allowing electrical communication with said programmable element through said first pad before packaging said circuit, wherein a conductive path from said first pad to said element is free of regulation by any transistor; and
preventing all electrical communication to said programmable element through said first pad after packaging said circuit.

48. The method in claim 47, further comprising preventing at most some electrical communication with said latch through said first pad before packaging said circuit.

49. The method in claim 48, further comprising allowing electrical communication with said programmable element through said second pad, wherein a conductive path from said second pad to said element is regulated by at least one transistor.

50. The method in claim 49, further comprising allowing electrical communication with said programmable element through said second pad after packaging said circuit.

51. The method in claim 50 further comprising preventing all electrical communication with said latch through said first pad after packaging said circuit.

52. The method in claim 51, further comprising avoiding electrical communication with said programmable element through said second pad before packaging said circuit.